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Automotive apps are driving inspection requirements for advanced nodes

Chip Scale Review asked KLA-Tencor experts Jeroen Hoet and Stephen Hiebert to respond to questions that provide insights into the defect reduction strategies needed for packaging of devices intended for automotive applications.

CSR: How is the defect reduction strategy for packaging at outsourced semiconductor assembly and test suppliers (OSATS) or integrated device manufacturers (IDMs) different for the automotive industry compared to other industries such as consumer or mobile?

KLA-Tencor: At the final packaging assembly and test stages we see various trends for automotive that differ from consumer and mobile applications. Because of the push of the automotive industry for "Zero Defects," increasing reliability is a higher priority than reducing package size for automotive applications. Therefore, well-proven packages dominate this market, for example, leaded-packages like quad-flat package (QFP) and also ball grid array (BGA), or quad-flat no-leads (QFN) packages.

The most common package type in use today for automotive applications is the leaded-package. In the past, there was little economic incentive to focus on process control and defect traceability in the assembly lines. "Zero Defect" is changing this paradigm. A new focus on ensuring all contact points (wings for gull-wing leads) are within the dimensional tolerances will help to identify defects that create shorts or otherwise decrease the assembly quality. Each component that does not meet the tolerances will be sorted out of the production stream and will not make it to the customer. In addition to the increased inspection requirements, automotive customers are introducing additional package cleaning steps, with brush cleaning devices or CO_2 cleaning, to further reduce the number of failed packages that are shipped. Examples of burr and dirt-on-lead (DOL) defect images on leaded devices are in Figure 1. After defect detection, these parts can undergo a cleaning step to remove the dirt from the leads and increase the yield.

As the market requirements have grown, the ICs packed inside the packages noted above have increased their memory content and clock speeds, resulting in increased complexity. For this reason, the share of BGA packages is growing faster than the leaded-components on account of the higher density of available contact points compared to gull-wing packages. Similar to the trend with leaded-packages, BGA components for automotive applications also have increased inspection requirements with tighter specifications for contact points' (solder balls for BGA) dimensions, and newly introduced cleaning techniques at the end of the line.

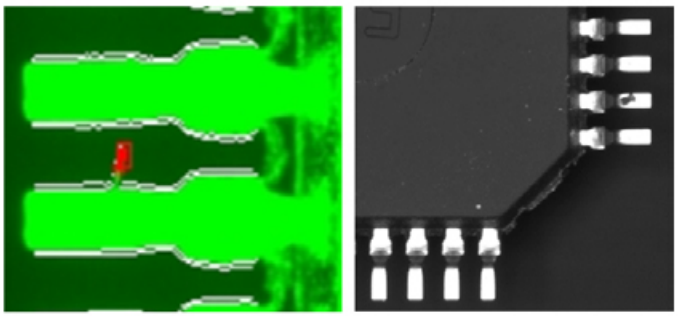

Figure 1: Examples of a) (left) burr and b) (right) dirt-on-lead (DOL) defect images.

Another trend is the increasing adoption of unique item level traceability (ULT), which guarantees that defects found at the end of the line are traced back to their origin. ULT allows a failure of a single IC inside a package to be traced back to the root cause of that failure at an earlier assembly step, or even at the wafer level. Reaching parts per billion reliability levels requires this kind of proactive defect reduction strategy that puts focus on all potential sources of failure.

CSR: How does the process control strategy at the packaging level change with the advent of system-on-chips (SoCs)/ICs in the 14nm and 10nm design rule range for automotive applications? What should the manufacturers at the packaging level do differently that they didn't need to worry about with respect to design rules >65nm.

KLA-Tencor: Even at the less advanced nodes, all automotive chip manufacturing process flows already contain significantly more inspection and metrology steps than found with consumer devices. These additional steps help recognize manufacturing excursions faster, improve the traceability of the source of the problem and keep non-conforming material out of the supply chain. This strategy requires automotive suppliers to focus on the wafer level and the packaged IC to find and eliminate defects at the source, as well as screen the production work in process (WIP) to prevent any defect excursions.

The process control strategies noted above have become even more stringent for design rules below 65nm. At the 1Xnm nodes, the transistor and metal layer dimensions have scaled down to such an extent that cross-talk and large on-chip interconnect parasitics (resistance, capacitance and inductance) have become significant issues. To resolve these undesirable characteristics, low-k SiO_2 doping is used to improve the performance of the interconnects to retain a high clock-speed, lower cross talk, reduce time delays and lower power consumption. However, because low-k dielectric material is more brittle than conventional oxides, there is an

increased risk of die cracking during the wafer dicing step (see **Figure 2**).

As a consequence of the increased risk of die cracking during the dicing step, manufacturers for the automotive industry are facing an increased need to add die crack inspection at the final die sorting step to guarantee cracked devices are removed from the line. The absence of e-test after dicing puts a priority on detection of these killer defect types through inspection techniques. Many of the side wall cracks capable of impacting the active area and destroying the device are also invisible to standard optical inspection. Infrared radiation (IR)-based technologies are currently being investigated to close the inspection gap. It is already demonstrated that an inspection with an IR camera directly above the device on the wafer does not provide the required sensitivity to detect the small side wall cracks. An innovative IR-based inspection solution has been developed to maintain sensitivity to all sides of the device. This new technology has already proven to provide zero slip-through in high-volume production. The key challenge is to maintain the required sensitivity at high-volume manufacturing (HVM) speeds of >8K dies/hour to guarantee an acceptable cost of ownership. Only limited suppliers are currently capable of offering zero underkill crack inspection at HVM-worthy speeds.

Many other changes in process control strategies can be found in wafer-level packaging. As 14nm and below semiconductor front-end technologies get deployed for automotive applications such as artificial intelligence (AI) and advanced driver assistance systems (ADAS), highly advanced packaging applications will also be utilized to enable very high bandwidth. Innovative 2.5D, 3D-IC, and high-density fan-out packaging technologies will be required for the electronics systems to process very large volumes of data in real time. Shrinking chip interconnect pitch and scaling redistribution layer (RDL) dimensions drive requirements for higher resolution inspection and high-accuracy metrology at the wafer level. Resolution of inspection and accuracy of metrology will both be pushed to sub-micron levels. These advanced packaging technologies also have many more process steps than established automotive packaging technologies, and this process complexity drives significant inline inspection and metrology to achieve yield, quality, and reliability necessary for automotive deployment.

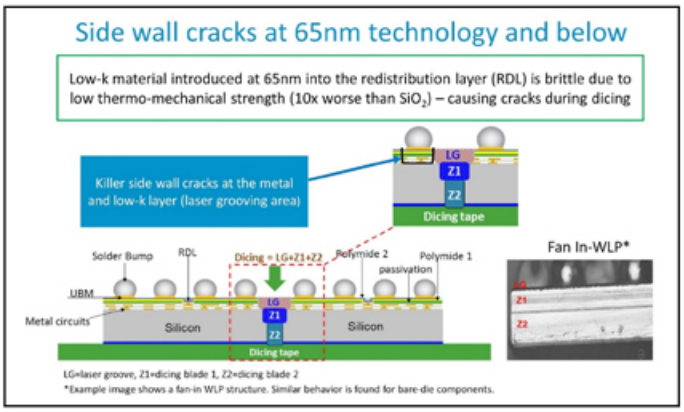

Figure 2: Side wall cracks at 65nm technology and below.

CSR: How do you foresee reaching parts-per-billion (ppb) automotive quality levels as the industry continues to need to provide ICs at ever smaller design rules? Another consideration could be that as the number of ICs being incorporated into autos continues to grow — that will also impact the level of reliability needed because the greater the number of ICs in a system, the higher the probability of failure unless the reliability of each IC can be improved.

KLA-Tencor: As the semiconductor content in luxury vehicles grows beyond 10,000 devices, the cumulative effect of semiconductor reliability is the top issue for the industry. Semiconductors have already become the #1 failure item in car quality, with the challenges continuing to grow. The difficulty in meeting ppb quality targets cannot be overstated. Leading automotive suppliers today can reach quality levels in the 1-10ppm range on mature devices that are built on well-characterized, larger design rule processes that have been in production for many years. Making the desired orders of magnitude improvements in quality cannot be accomplished by simply massaging the margins of these processes. Rather, it will require a fundamental rethinking of quality methods, business models and capital investment.

Compounding this reliability challenge is the rapid push of more advanced design rule devices into the automotive supply chain. Whether in AI chips for autonomous driving, domain controllers replacing traditional distributed electronic control units (ECUs), or advanced ADAS chips and sensors, the raw computational requirements are driving these advanced parts into cars. Car manufacturers will be faced with a significant reliability hurdle because these devices are more complex, far less mature, and difficult to test. Because reliability affects both warranty and liability, as well as the brand image of car manufacturers — and potentially the safety of their customers — process control in packaging, from wafer level to component, will increase significantly in the coming years to find and eliminate the sources of defects and screen for excursions. Manufacturers must seek every available opportunity for continuous improvement across the entirety of their manufacturing process to reach the goal.

Biographies

Jeroen Hoet received his Executive MBA from Vlerick Business School, Belgium, his MBA from U. of Leuven, Belgium, and an MSc Engineering in Micro-electronics from Ghent U., Belgium. He is a Product Marketing Manager at KLA-Tencor; Jeroen.Hoet@kla-tencor.com

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